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DSP VALLEY newsletter 3

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In this issue

MiPlaza automated setup enables RF on-wafer measurements with short throughput time for NXP project

MiPlaza (Microsystems Plaza) offers leading edge research services and shared access to state-of-the-art research infrastructure. MiPlaza is part of Philips Research and provides these services to high tech organizations inside and outside Philips.

MiPlaza

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MiPlaza automated setup enables RF on-wafer measurements with short throughput time for NXP project

Located at the High Tech Campus Eindhoven, MiPlaza's expertise includes multi-purpose cleanrooms for thin film processing and systems-in-package, prototyping and systems creation, materials analysis, and electronic test and measurement.

One of the most recent additions to MiPlaza's capabilities is the Electronic Measurement Laboratory (EM-lab), set up in partnership with Agilent Technologies and Cascade Microtech.

In a joint project/cooperation, MiPlaza's EM-lab and NXP-ICLab. investigated automated high frequency on-wafer measurements to characterize a wide-band preamplifier designed by ICLab. The preamplifier is part of a transceiver[1]. The S-parameters, noise figure and linearity parameters of the integrated preamplifier were measured at different bias settings over the entire 200mm wafer.
These measurements where performed in collaboration with Agilent Technologies.

This article describes the capabilities of the semi automated RF on-wafer set-up and shows some measurement results.

About the preamplifier and probing

Figure 1 shows the layout of a stand-alone version of one of the integrated low-power (1.8V/2mA) high-gain preamplifiers, which are designed for UWB wireless applications (7 – 8 GHz). To allow quick and easy probing of the preamplifier a template for wafer probing has been defined for on-wafer characterization.

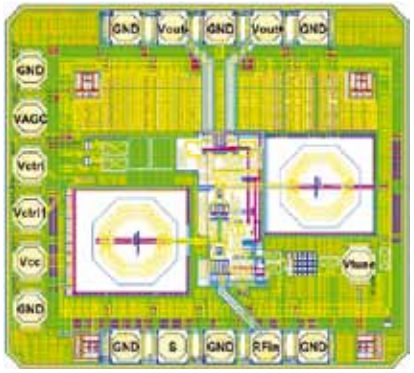


Figure 1, Die layout of preamplifier

On-wafer measurement setup at the MiPlaza EM-lab in Eindhoven

The characterization setup at the MiPlaza EM-lab in Eindhoven is shown in Figure 2 and 3. The set-up can handle complete 300 mm wafers and includes a thermo chuck with a sweep range from -55 to 200°C. All system components, network analyzer, prober, semiconductor parametric analyzer are computer controlled, enabling the measurements to be fully automated. This is a key benefit for throughput time as many parameters on several dies and sub dies had to be tested under 40 different power supply conditions. Performing this manually would have been very time consuming and prone to errors.

Measurement equipment

The Agilent PNA-X network analyzer [2] was used for S-parameters, Inter Modulation Distortion (IMD), compression and noise figure measurements. The measurement concept used in this network analyzer (cold noise technique [3]) makes on-wafer noise measurements much simpler than the classical Y factor method (no noise source connection required at the input of the DUT). Flexible internal switching and multisource capability in the instrument enables all these measurements to be performed at once with one connection to the DUT. The B1500 [4] parametric analyzer was used to apply the different power supply voltages and to accurately measure the total current through the circuit.

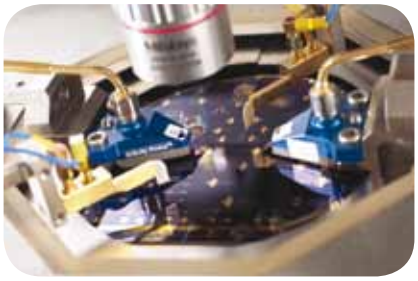


Figure 2. Prober+instrumentation

Figure 3. Probing

(1) Y. Dong, Y. Zhao, G. van Veenendaal"A 9mW high band FM-UWB receiver front-end", IEEE Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European 15-19 Sept. 2008 Page(s):302 – 305
(2) AGILENT link, www.agilent.com/PNA-x
(3) AGILENT link, www.agilent.com/PNA-X Source-Corrected Noise Figure Measurement (Option 029)
(4) AGILENT link, www.agilent.com/B1500

Some measurement results

Examples of the generated measurement results are presented in Figure 4 and Figure 5. Figure 4 shows S21 as function of frequency for 1 bias setting. Figure 5 shows the noise figure (NF) as function of frequency for 3 bias settings of the preamplifier.

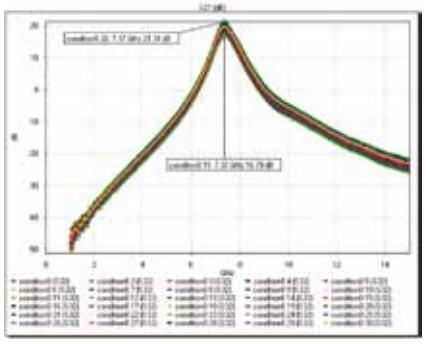


Figure 4, Measured S21 as function of frequency for 1 bias setting

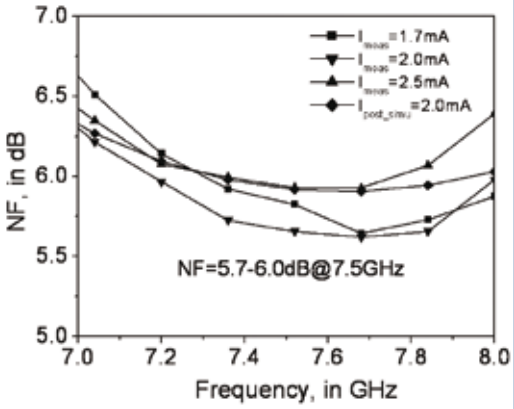


Figure 5. Measured NF at different bias settings of the Pre-amp

Conclusion

The MiPlaza EM-lab supported NXP-ICLAB with full on-wafer RF characterization of preamplifiers. The preamplifiers were supplied on an 8 inch wafer containing 69 dies. Each die containing 8 preamplifiers, so approximately 552 circuits were probed in total. This resulted in roughly 11000 measurement results (files) acquired in a very short throughput time of only 1 week. Manually, the throughput time would have been some months.

MiPlaza is currently assessing extending the EM-lab with "Virtual Lab" capabilities that would allow customers to access the EM-lab capabilities on-line from their own desk, anywhere in the world. ■

Sigasi Enters EDA Market with Public Beta Program

Sigasi
automated hardware refactoring

Program makes Intelligent Development Environment available to VHDL designers

Sigasi, an early stage EDA company, announced the launch of a Public Beta Program for Sigasi HDT, an Intelligent Development Environment (IDE) for VHDL.

Sigasi HDT offers a smart and comprehensive design platform for VHDL. Building upon the widely accepted Eclipse platform, it contains an ultra-fast VHDL parser and compiler which run transparently in the background. The tool fully understands the complete design in terms of VHDL concepts, allowing the digital designer to make modifications faster and smarter. *"This technology enables a wide range of innovative features, such as intelligent navigation, instant error reporting, code completion and code refactoring"* said Sigasi's CTO Hendrik Eeckhaut.

Hendrik Eeckhaut

Public Beta Program

Sigasi HDT has already been extensively tested with early adopters. Through the Public Beta program, Sigasi will build a community of hardware designers that take advantage of modern development techniques.

To participate in the program, users should visit http://www.sigasi.com/sign-up.

Business Benefits

Sigasi HDT significantly increases design productivity for both occasional and experienced VHDL designers, by helping them to write, inspect and reuse their designs in an intuitive way.

Philippe Faes

"Our technology is inspired by the most advanced software development environments, but it is unique in the hardware design world", said Philippe Faes, Sigasi's CEO. *"Operations that may take hours when done by hand, can be done in minutes with our tool."*

■

About Sigasi

Sigasi is an early stage Electronic Design Automation (EDA) company and focuses on the creation of an Intelligent Development Environment (IDE) for Hardware Description Languages (HDLs). Sigasi HDT drastically increases the productivity of hardware designers by helping them to write, inspect and reuse their designs in an intuitive way. The company is headquartered in Ghent, Belgium. For further information, please visit http://www.sigasi.com.

AnSem developed a low power ADC for smart sensor network applications

The evolution towards wireless, wearable and intelligent personal networks has only gained interest in the past few years. This tendency is growing and can be seen everywhere, from the consumer and medical markets to the industrial and automotive worlds.

For these kinds of applications, it is of uttermost importance to smartly design all the different building blocks inside the complete system. Only then, the total power budget can be minimized, allowing a longer battery lifetime, or even enhancing "battery-less" operation.
Sensor networks all need an interface between the real - analog - world and the digital processing core of the system. This makes the use of an analog-to-digital converter (ADC) essential.

Depending on the signal you want to monitor in your network, the ADC will have different requirements. For medical applications, like for example in Body Area Network (BAN), most signals have a low frequency content. The ADC sample rate can therefore greatly be reduced, saving up substantial power.

AnSem has developed an ultra low power ADC with a 14-bit resolution and a sample rate of 2.5 ksamples/sec. It is a cyclic ADC using a RSD (redundant signed digit) technique for offset cancellation. The total power consumption is 40 µA, with a supply of 2.5V. The cyclic architecture offers a dramatic reduction in silicon area, compared to alternatives, which allows its use in miniaturized or even implantable systems. The topology also features self trimming, which increases performance even further.
This ADC is available in several technologies. A rescalable approach allows easy reuse and modularity to build a new system quickly and efficiently. ■

Hightech in the Solar Car

A Look behind the Solar Screen

In October 2007, the Solar Team of GROUP T-Leuven Engineering College finished second in the Panasonic World Solar Challenge, the world championship for solar cars in Australia. The team designed and built, especially for the race, a unique Solar Car. The contest and the team were already extensively covered in the media but what exactly goes on behind these shimmering solar panels? We talked to Brecht Van Hooreweder, Electromechanical engineer and the person responsible for the Frame & Design of the second Solar Team. His work was awarded with the Agoria Thesis Award. This employers' organization represents the Flemish technological industry sector.
The Solar Car of the Leuven engineering students not only looks spectacular, it is most of all an extraordinary example of technological ingenuity. A couple of numbers to illustrate. On an average summer day the car can easily reach 130 km per hour. With a CdA of less than 0.095, its air resistance is 6.25 times less than a Porsche Carrera. Its electrical engine has an efficiency of 95%; this is twice that of a gasoline engine. The car weighs only 195 kg, while it measures 5 m in length, 2 m in width and 1 m in height. To compare: a small Peugeot 206 weighs 5 times more.

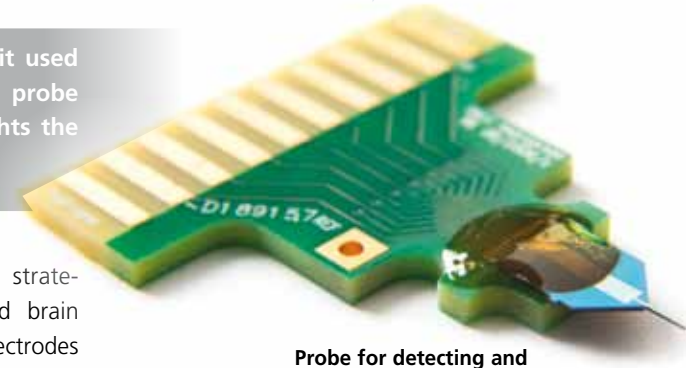
GROEP T LEUVEN HOGESCHOOL

Super light and strong as heck

One of the greatest challenges of the Solar Project was the design of the lightweight chassis, or the carrying structure of the car. *"You can compare it to the human skeleton"*, says Brecht. *"The chassis ensures the rigidity and the strength of the whole. All parts are attached to it. The carrying structure of the car must also be able to absorb all the forces that result from braking, accelerating and taking a corner. Also, the safety of the pilot must be guaranteed by the carrying structure. The challenge consisted of designing a super-light yet very strong structure."*

IMEC's design strategy for brain implants paves the way to multi-electrode deep-brain stimulation

IMEC presents a new design strategy for brain implants, which it used to create a prototype multi-electrode stimulation & recording probe for deep-brain stimulation. With this development, IMEC highlights the opportunities in the healthcare market for design tool developers.



Probe for detecting and stimulating individual brain cells

Brain implants for electrical stimulation of specific brain areas are used as a last-resort therapy for brain disorders such as Parkinson's disease, tremor, or obsessive-compulsive disorder. Today's deep-brain stimulation probes use millimeter-size electrodes. These stimulate, in a highly unfocused way, a large area of the brain and have significant unwanted side effects.

Wolfgang Eberle, Senior Scientist and project manager at IMEC's bioelectronics research group: *"To have a more precise stimulation and recording, we need electrodes that are as small as individual brain cells (neurons). Such small electrodes can be made with semiconductor process technology, appropriate design tools, and advanced electronic signal processing."*

IMEC's design and modeling strategy allows developing advanced brain implants consisting of multiple electrodes enabling simultaneous stimulation and recording. This strategy was used to create prototype probes with 10 micrometer-size electrodes and various electrode topologies.

The design strategy relies on finite-element modeling of the electrical field distribution around the brain probe. This was done with the multi-physics simulation software COMSOL 3.4 and 3.5. The COMSOL tools also enabled investigating the mechanical properties of the probe during surgical insertion and the effects of temperature. The results indicate that adapting the penetration depth and field asymmetry allow steering the electrical field around the probe. This results in high-precision stimulation. Also key to the design approach is developing a mixed-signal compensation scheme enabling multi-electrode probes capable of stimulation as well as recording. This is needed to realize closed-loop systems. These new design approaches open up possibilities for more effective stimulation with less side effects, reduced energy consumption due to focusing the stimulation current on the desired brain target, and closed-loop control adapting the stimulation based on the recorded effect. ■

"In the first designing phase, we opted for using thin-wall aluminum profiles", Brecht continues. *"These combine precisely a high strength and rigidity and a light weight and, consequently, are very suitable for the carrying structure of the solar car. We also looked for a special kind of aluminum that can be easily welded. This way, the profiles can be easily connected with each other in a solid structure at the assembly of the chassis."*

Super fast but not perfect

Once the profiles were chosen, the search was on for its optimal position in the aerodynamic bodywork. *"This phase of the design process was the most complex but also the deciding factor in the development of the carrying structure"*, Brecht confirms. *"We used specialized software that is only used in a few companies in the world. In professional terms this is called 'optimization software'. With it, you can calculate the position of the different profiles within the aerodynamic bodywork. After all, we were looking for the optimal distribution of the material to achieve a lightweight structure that is exactly rigid and strong enough to resist all forces acting on it."*

But this was the problem. The software may very well work super fast but you cannot expect a miracle solution from

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Using an Eclipse-based IDE for Embedded Development

expresslogic

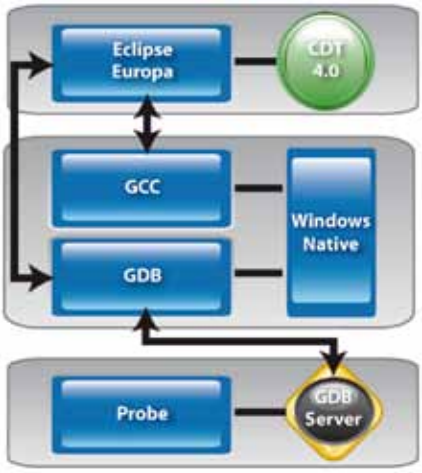
The open-source Eclipse movement has become a major factor in the software industry largely because it offers developers a free comprehensive Integrated Development Environment (IDE) and the ability to take advantage of a large number of free or inexpensive add-in productivity tools.

Eclipse was established by IBM to foster development of applications based on Java. Embedded developers, however, need capabilities not found in Eclipse. For an embedded developer to use Eclipse, the gap between Java-based enterprise development and the embedded world have to be bridged. Embedded development is generally done in C with some assembly; the code is typically cross compiled and executed on an external target computer board. Getting the program onto the board requires some type of a host-target connection. While debugging, detailed CPU register and memory information, RTOS state information is generally helpful to the embedded developer. While the Eclipse C/C++ Development Toolkit (CDT) includes support for C and C++ it requires the user to switch back and forth between the C/C++ and the Debug "perspectives".

The Need for a Low-Cost Commercial Eclipse-based Solution

Commercial offerings of Eclipse-based IDEs generally are priced at the same level as proprietary IDEs, which is understandable, since vendors derive their revenue from the sale of licenses to use their tools. While enterprise versions of Eclipse and CDT are free, there is a high price required for an IDE that is well suited to embedded development.

Believing the industry would benefit greatly if there were an Eclipse-based solution that addressed the needs of embedded developers, but was as affordable as the open-source Eclipse itself, Express Logic developed the BenchX® product. The BenchX IDE combines an embedded-optimized Eclipse IDE, GNU C/C++ compiler and toolchain, and a host-target debug probe in a complete, integrated, and commercially supported package.



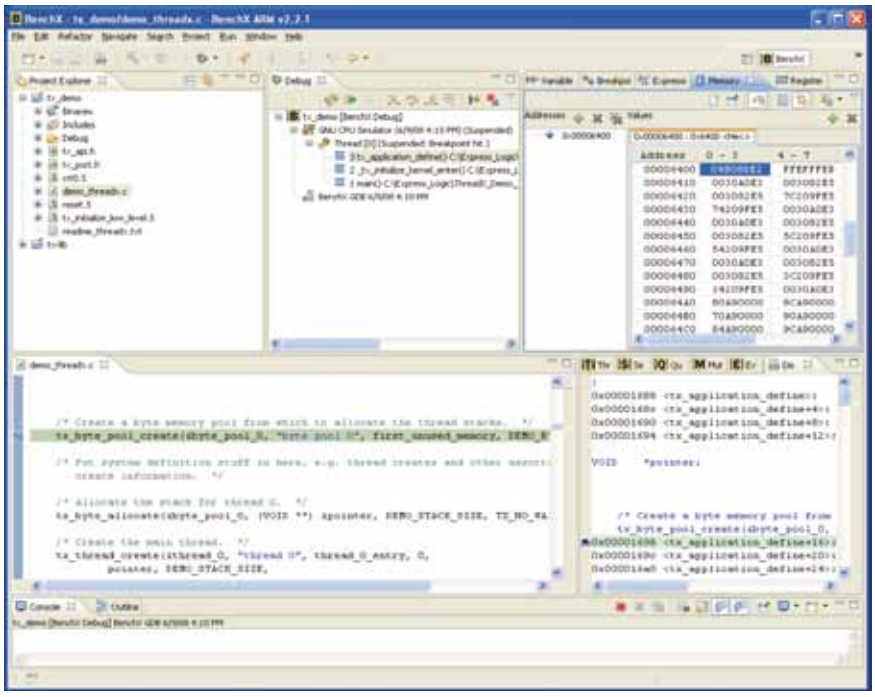
Tailored to meet the needs of embedded development

In BenchX, the GNU tools are integrated into the Eclipse Project Builder. The GDB debugger is seamlessly integrated with the CDT debugger GUI and the target debug probe, providing the ability to control the execution of target-resident application programs from a user-friendly GUI on the host.

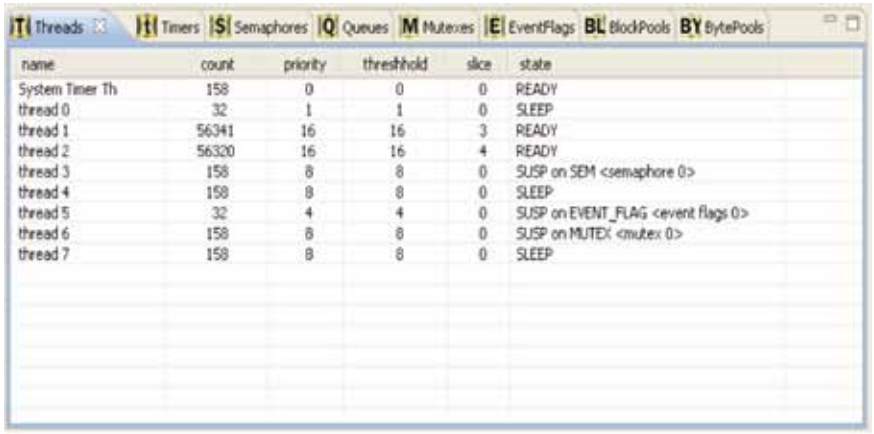
A single BenchX Perspective provides access to all the views and tools necessary to create, edit, assemble, compile, link, locate, execute, and debug an embedded application. The figure below shows the debugger in action.

The BenchX debugger also includes a capability critical for embedded development – RTOS kernel awareness. With no real counterpart in the enterprise world, it's not surprising that Eclipse does not have the ability to assist the developer in viewing RTOS kernel objects of interest, such as threads, semaphores, and queues.

Even with the many changes that make it more suitable for embedded development, because BenchX adheres strictly to the Eclipse interface standards, it may



be enhanced through the addition of Eclipse plug-in tool components such as compilers, text editors, and static analysis tools. Users can take full advantage of over one-thousand Eclipse plug-ins available to improve development productivity (see: http://www.eclipseplug-incentral.com/ for a complete list of available plug-ins). As a result, BenchX provides a simple yet fully modular foundation that is open for upgrade and expansion thanks to its Eclipse heritage.



name	count	priority	threshhold	slice	state
System Timer Th	158	0	0	0	READY
thread 0	32	1	1	0	SLEEP
thread 1	56341	16	16	3	READY
thread 2	56320	16	16	4	READY
thread 3	158	8	8	0	SUSP on SEM <semaphore 0>
thread 4	158	8	8	0	SLEEP
thread 5	32	4	4	0	SUSP on EVENT_FLAG <event flags 0>
thread 6	158	8	8	0	SUSP on MUTEX <mutex 0>
thread 7	158	8	8	0	SLEEP

Authors

John A. Carbone, vice president of marketing for Express Logic, has 35 years experience in real-time computer systems and software, ranging from embedded system developer and FAE to vice president of sales and marketing. Prior to joining Express Logic, Mr. Carbone was vice president of marketing for Green Hills Software. Mr. Carbone has a BS degree in mathematics from Boston College.

Stefaan Kiebooms, senior software engineer for Express Logic has 15 years of extensive experience in debugging and improving embedded software products, ranging from custom projects, to IDEs, compilers, debuggers and RTOSes. Stefaan has a Masters in Computer Science from K.U.Leuven university. ■

Preface

DSP Valley: network or cluster? (or both?)

For the European Commission, clusters are a very strong element in regional development. In this context, it is useful to ask whether DSP Valley is a cluster.

Since its foundation, now more than 12 years ago, DSP Valley has always profiled as a technology network, with a thematic focus on the design and development of embedded signal processing technology, and with the objective to stimulate new innovative partnerships. This technology focus and objective are still valid today, and especially the objective of partnering and matchmaking is even more valid than ever before. This is implemented through the organization of numerous matchmaking and brokerage events, with European inter-cluster B2B matchmaking as the newest addition to the successful networking events of DSP Valley.

Because of the strong focus on this matchmaking and partnering aspect, DSP Valley is indeed instrumental in stimulating and creating new cooperation. As a result, today all members of DSP Valley have partnership with several other network members. Therefore the industrial and academic members of DSP Valley have established a strongly linked and interconnected ecosystem. Based on these very intensive interconnections, the group of companies and research institutes participating in the DSP Valley network, have also established a very strong cluster.

Today, DSP Valley still is a network, and will remain a network, and will continue to offer networking services and activities. But the main result of this networking is cooperation amongst the network participants. Is DSP Valley a network or a cluster? DSP Valley is very proud to be both!

Regards,
Peter Simkens
Managing Director
DSP Valley

Dual-constellation live L5 tracking with Septentrio PolaRx3G

With the launch of the first GPS satellite transmitting signals on L5, researchers and other GNSS specialists interested in evaluating and monitoring GPS and Galileo signals on 2 common frequencies, can now perform tests with live signals from both constellations on L1 and L5/E5a using off-the-shelf commercial GNSS receivers from Septentrio.

Septentrio receivers are successfully tracking the new L5 signal transmitted from GPS satellite SVN49. This IIR-M satellite was launched on March 24 2009 and carries a demonstration payload capable of transmitting the new L5 signal, in addition to the standard L1/L2 payload. The satellite started transmitting in the L1 and L2 band on March 28, shortly after having been boosted to its quasi-circular orbit. The turn-on of the demonstration L5 signal occurred on Friday April 10 around 11:58 UTC.

Septentrio CEO Peter Grognard comments: *"Septentrio engineers have closely been following the commissioning of this particular satellite, from its launch to its first L1/ L2 transmissions, up to its first transmissions in the L5 band. We are proud to offer our customers the opportunity to be a part of this historical step in GNSS signal availability."*

Septentrio receivers are now successfully tracking a total of 5 signals broadcast by SVN49: L1-CA, L1-P(Y), L2-P(Y), L2C and, last but not least, L5. Septentrio offers its customers a special firmware adapted to track the L5 test signal on the standard commercial platform PolaRx3G.

Construction GSP IIR-M satellite. Lockheed Martin photo.

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it. *"In fact, the software applies exactly the same formulas as an engineer would but much faster"*, says Brecht. *"What it comes down to is that the user must first enter all data and preconditions, like a three-dimensional drawing of the chassis, the forces affecting the structure, the material properties, etc. Based on this, the software then suggests the optimal position of the profiles."*

Supplementary control

But, as mentioned before, this is where the limitations are found. For the computer takes into account only the data entered by the user. And that is never 100% correct. *"Consequently, a meticulous verification of the solutions offered by the software were required"*, according to Brecht. *"This was done by classic manual calculations. We also tested some welded aluminum test bars in order to verify their material properties and the strength of the weld. Furthermore, we also studied the practical feasibility of the material distribution. For instance, the software can theoretically have five profiles come together in one point while in practice a maximum of three can be connected. To that end, we built a full-scale wooden prototype of the carrying structure. This way, we could trace potential problems with the production of the structure at an early stage before they surfaced on the welding table."*

Additionally, these same receivers are capable of tracking Galileo signals in the L1 and L5-band as well, offering opportunities for the first ever dual-frequency GPS/Galileo trials using signals in the same frequency bands. Dr. Hans van der Marel from Delft University of Technology, The Netherlands, comments: *"It is very useful for researchers like ourselves to be able to simultaneously collect L1/L5 GPS and L1BC/E5a GIOVE measurements. During the previous night, we tracked a complete pass of GPS SVN49, together with GIOVE-A and GIOVE-B, and are excited to analyze one of the first datasets including both GPS L5 and GIOVE-A/B E5a measurements. One of our first observations is that the power of the demonstration GPS L5 signal is even higher than expected when the satellite is in the zenithal direction, while the opposite is true at lower elevations."* ■

About Septentrio

Septentrio Satellite Navigation NV designs, manufactures, markets and supports high-end OEM GNSS receivers for demanding professional navigation, positioning and timing applications. Septentrio has an international team of experts in all areas of satellite navigation receiver design and applications. For more information about Septentrio, please visit our website at www.septentrio.com.

Samsung Electronics joins IMEC research program on green radios

25 imec Years of Making Technology Fly

Samsung Electronics signed a Memorandum of Understanding with IMEC to lay down their intent to collaborate on technologies for green radios. The research collaboration topics will include cognitive reconfigurable radio baseband and millimeter-wave wireless communications technologies.

Building on its expertise in software-defined radios that support the major standards for wireless communications, IMEC pushes its research one step further towards cognitive radios (ICs with a radio that adapts itself to the changing environment, not only to the communication standard, but also to the available communication frequencies and conditions such as indoor/outdoor, signal strength, movement). IMEC is working on the control algorithms that take into account these changing environment parameters and user needs. As another cornerstone of its research into wireless communication, IMEC develops radio ICs for the wireless communication of massive data

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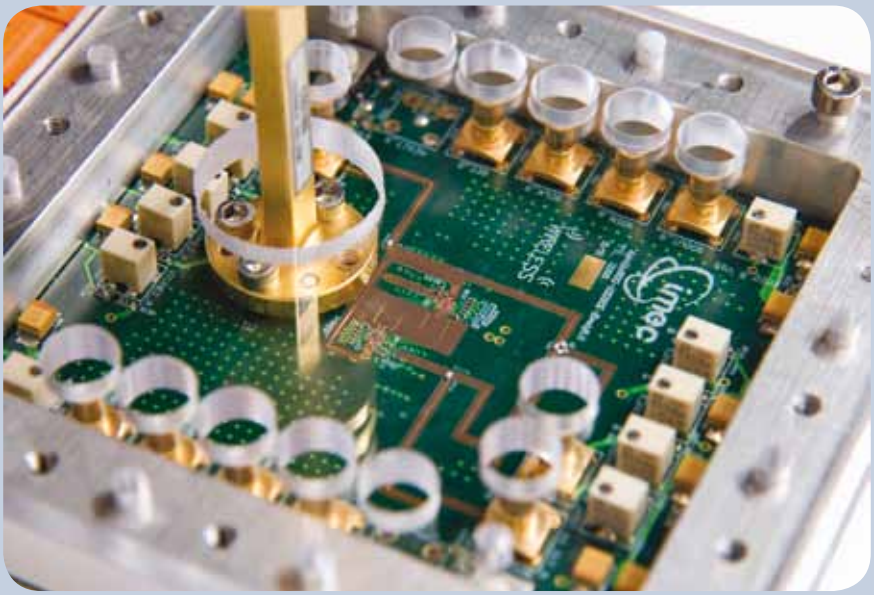


Integration photo of IMEC's 45nm RF front-end IC with antenna and antenna interface for 60GHz communication

Proof of quality

The design of the carrying structure took two full months. The production itself only took three weeks. The chassis of the solar car has now gone through 10,000 km – of which 3,000 through the rough Australian desert – and it still meets all quality demands. *"The specialized optimization software has proven its value. Our solar car was effectively one of the lightest of all contestants in the World Solar Challenge 2007. However, we can say that without the additional verification calculations and tests we wouldn't have been able to design a chassis that was both light and reliable and was easy to produce"*, Brecht believes.

That Brecht's design work also attracted a lot of attention internationally appeared from the large turnout for his lecture during the World Automotive Congress Fisita in Munich from 14 to 19 September 2008. This is just about the most important trade fair in the automotive sector.

In July 2008, a new Solar Team fired up at GROUP T. The team members won't go to Australia for less than a first place next year. *"Our design results will be of good use to them"*, Brecht concludes. (See also article 'New Solar Team is going for Gold' on page 10)

■

GROEP T LEUVEN HOGESCHOOL

World Solar Challenge 2009 in the making
NEW SOLAR TEAM IS GOING FOR GOLD

GROEP T LEUVEN HOGESCHOOL

An eleventh place in 2005, second in 2007 and in 2009 ... 1st place! The fourteen students of the GROUP T Solar Team are brimming with self-confidence. The experience, the expertise and the extensive network of contacts that has been established over the past years in addition to a youthful exuberance and team spirit give them wings.

Team leader Thomas Teirlinck and marketing manager Toon Reynders are very much aware that the expectations are high. *"The many companies that support and sponsor us, our university college, the press, our friends and sympathizers, the audience at large ... everybody expects that we will triumph next year in Australia,"* Thomas confirms. *"The competing teams of course take that into account. Where before, they hardly noticed the 'little' Belgians, they now realize a fearsome adversary is coming."*

The World Solar Challenge is the unofficial world championship for cars powered by solar energy. The bi-annual contest is an exhausting race of 3,000 km straight through the Australian outback from Darwin in the north to Adelaide in the south across the barren desert. *"Teams from all around the world participate in this contest, usually from prestigious, big name universities like the Massachusetts Institute of Technology, Stanford University, Michigan University and – last but not least – our eternal rival, the Technische Universiteit Delft,"* Toon explains. *"That is the team to beat. It will not be the easiest thing since we are a comparatively small team with limited means. If you see the budgets of the American teams that are sponsored by the large multinationals, our possibilities are rather modest. Still, the previous Solar Team left the American mastodons behind. The only thing left now is to beat the Dutch and our goal is accomplished."*

Solid training

The third Solar Team started in July 2008, immediately after the exams. *"We have thoroughly examined the approach and the method of the previous teams,"* Thomas tells us. *"In doing so, we have reached the conclusion that we need a different approach to a number of things; the preparation, to begin with. We immediately started with a solid technical training of the team members. We took professional courses on aerodynamics, finite elements, CAD, programming and so on with a specialized company. To that end, we went to Germany and France, among other places. A company like Altair organized training especially for us called 'optimizing based on finite elements'."*

"While the previous team launched themselves right into the concept phase and didn't take any training until later, we decided to do it the other way around," Toon continues. *"This ensures that we are more thoroughly prepared and that we can make better, theoretically sound decisions. This also means that we can do most of the research ourselves and do not need to delegate it to companies or research centers. This way we not only gain time but we also keep the entire production process under better control."*

A second change is the concept phase itself. *"We want to extend and intensify it,"* Thomas clarifies. *"With respect to aerodynamics, controls and suspension, we will conduct increasingly thorough research. The same is true as regards electronics. While in the previous team there was only one real electronic engineer, seven more have now joined the club. Of course, that affects the way we work."*

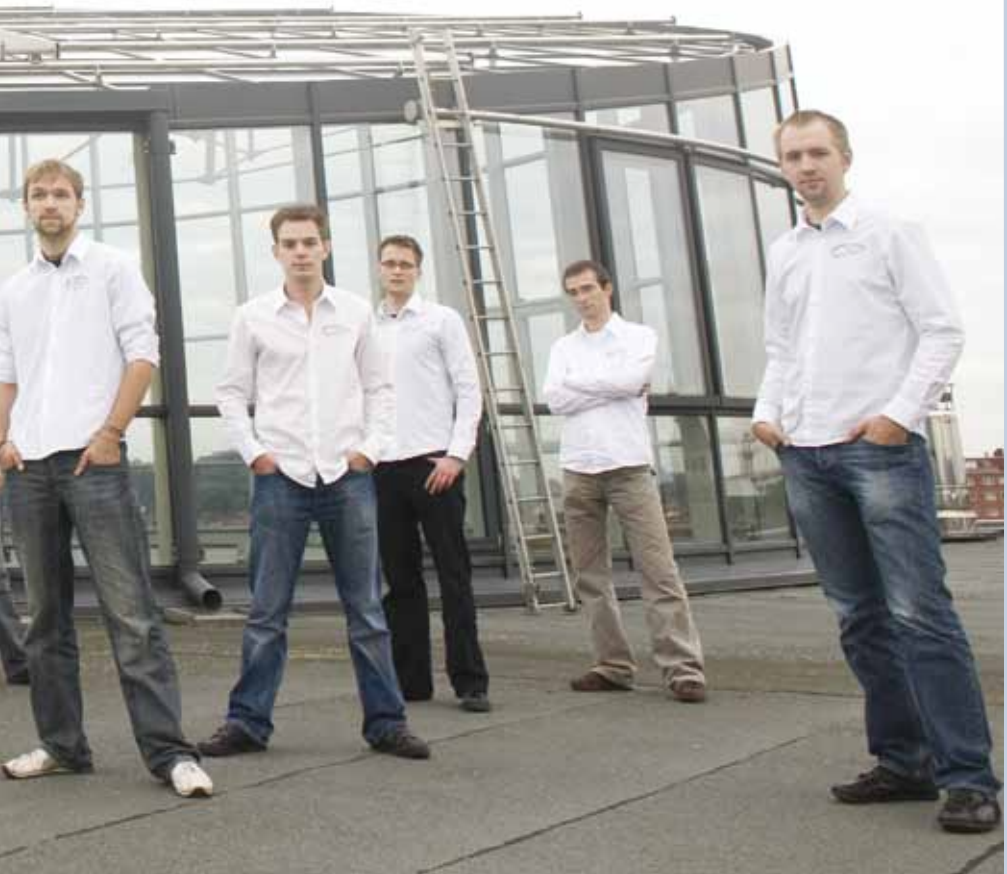
Three subteams

As regards organization, the Solar Team has maintained the structure of its predecessor. At the head is a team leader who coordinates three subteams. They are in charge of energy, mechanics and marketing, respectively. Toon has the following to say on this: *"The energy team is in charge of the energy supply of the car. These people have to take care of the maximum efficiency of the solar cells and their optimal positioning on the car. The energy team is also responsible for the development of the race strategy, a factor that can decide victory or loss. The mechanics team designs the construction of the car. They handle aerodynamics, the chassis, the suspension and finally the construction of the solar car itself. The marketing team, finally, manages the finances, looks for sponsors, provides logistic support, does the PR and handles contacts with press and media."*

Less energy

The competition rules are for the most part identical to those in the previous edition of 2005, yet, according to Thomas, a number of not insignificant changes have been made. *"First of all, the participants must use a lighter battery pack which means that less energy can be stored. This in turn means that everything must be even more energy efficient and an even more sophisticated racing strategy will be required. We will really have to monitor second by second. Also, the tires must meet new regulations. No longer slick tires but profile tires with a groove. No doubt good for safety but, on the other hand, this results in a greater rolling resistance and therefore higher use of energy while we will be able to store less. In short, there will be intensive puzzling over it and lots of calculations. But we are ready for it; what's more, we are in full swing."*

■



continuation from page 9

streams, for example for uncompressed high-definition television streams. Such data streams require a high throughput, in the order of Gbits per second. A suitable bandwidth for that communication is available around 60GHz. Therefore, IMEC works on cost-effective, low-power 60GHz radio ICs in standard CMOS, targeted at the consumer market,

Samsung has been a strategic partner of IMEC since many years. In 2004, Samsung joined IMEC as core partner in the (sub-)32nm CMOS research platform followed by a core partnership in IMEC's multi-mode multimedia research program in 2005 and in IMEC's ubiquitous embedded systems research in 2007. By joining both research programs on cognitive radio and millimeter wave communications, researchers from Samsung will closely collaborate with IMEC's research team to build up fundamental understanding and develop robust solutions for the future wireless terminals supporting multi-standards.

"We are excited that Samsung is contemplating on extending its collaboration with us towards cognitive radios and millimeter-wave communications;" said Gilbert Declerck, CEO of IMEC. *"We have been collaborating very successfully since 5 years and have learned from each other in many ways. This extension proves that our wireless communications research gives valuable knowhow to the industry to develop their mobile terminals of the future."*

"We are expecting the differentiated technologies developed together with IMEC to be the key ingredients of Samsung's next generation mobile devices. ;" said Dr. Kim, Head of Digital System Research Center of SAIT.

■

25 imec Years of Making Technology Fly

GN ReSound Uses Target's Optimizing C Compiler Technology for its Hearing Instrument DSP

TARGET
THE ASIP COMPANY

Target Compiler Technologies, the leader in application-specific processor (ASIP) design tools, announced that GN ReSound, a world leader in innovative hearing instruments, is relying on Target as its supplier of a complete software development kit (SDK) with an optimizing C compiler, for its Coyote-3 low-power digital signal processor.

GN ReSound initially used Target's IP Designer product, to model the Coyote-3 architecture and validate the performance of Target's C compilation and instruction-set simulation technology for its DSP. Then, a processor-specific SDK was generated from this model, using Target's IP Programmer product. The resulting SDK is now in production use for the development and implementation of new advanced audio functions in high-end hearing instruments.

Peter Ulrik Scheel, Senior Vice President, Research & Development of GN ReSound commented, *"With Target's IP Designer we are able to continue being the innovator of hearing solutions achieving still higher user satisfaction and acceptance. Today's hearing innovations require more sophisticated audio algorithms, which we can now implement quickly on our DSP thanks to advanced C compiler technology. Target's C compiler has proven to generate code as compact as hand-optimized assembly code, thus preserving the power and area advantages of our low-power DSP architecture."*

Gert Goossens, Target's CEO, comments: *"We are delighted to work with companies like GN ReSound that develop groundbreaking hearing instrument algorithms and devices that improve the quality of life for people with hearing loss all over the world. We look forward to our ongoing cooperation, to further extend their hearing instrument DSP solutions for more performance without compromising the size and power requirements of these devices."*

IP Designer is a retargetable tool-suite for the design and programming of ASIPs. The designer can easily describe ASIP architectures with performance and energy characteristics that are superior to general-purpose processors or close to hardwired data-paths. Using the nML modeling language and the retargetable software development kit (including highly optimizing C compiler, cycle- or instruction-accurate simulator, and graphical debugger/profiler), one can explore and fine-tune the processor architecture and then generate low-power RTL and comprehensive verification suites.

IP Programmer provides a comprehensive SDK for an ASIP. The SDK includes an ISO C99 compliant, highly optimizing C-compiler, assembler, linker and full featured debugger/profiler. Additionally, simulation models for virtual prototypes are made available as part of the package. ■

About Target Compiler Technologies

Target Compiler Technologies is the leading provider of retargetable software tools to accelerate the design, programming and verification of application-specific processor cores (ASIPs). Target's IP Designer tool suite has been applied by customers worldwide for diverse application domains, including GSM, WCDMA and HSDPA handsets, VoIP, audio coding, automotive infotainment, ADSL and VDSL modems, wireless LAN, hearing instruments, image processing, video processing, and various control and interfacing applications. Target is a spin-off of the Belgian nano-electronics R&D center IMEC, is headquartered in Leuven, Belgium, with North American operations in Boulder, Colorado.

About GN ReSound

GN ReSound is a leading international supplier of digital hearing instruments and audiological diagnostics systems. Headquarters are in Copenhagen, main production in China, a components' factory in Denmark and development centers in Denmark, the US and China. GN ReSound is among the leading companies in the industry, with subsidiaries in 25 countries and distributors in 80 countries. GN ReSound has 3,300 employees. http://www.gnresound-group.com.

DSP Valley @ DATE 09

DSP Valley was also present at DATE 09 in Nice (France). Here we had a group booth with 4 DSP Valley members: Easics, IMEC, Q-Star Test and Sigasi.
DATE is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design. It puts strong emphasis on ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.
Next DATE will be in Dresden (Germany) from 8 to 12 March 2010. ■

Mind helps companies to implement open source technologies for multimedia streaming

mind
embedded development
an ESSENSIUM division

Streaming multimedia is used in many embedded devices today, like surveillance and security systems, home automation systems, residential gateways, telecommunication and traffic control systems. And this is probably just the beginning. In a growing number of markets, multimedia features are becoming key to differentiate from competition and win market shares.

However, building an embedded multimedia streaming application is not a simple task. It requires a thorough understanding of a number of technologies like codecs, network protocols, and synchronization, which are often not the core expertise of the companies that decide to embed multimedia in their products. Codecs come in a variety of flavors for the different compression standards available, like MPEG (1, 2, 4), H.264, Motion JPEG, and Theora. Each of these standards has its advantages and drawbacks in terms of video quality, bit rate, robustness, and HW/SW required.

The network protocol is typically RTSP (Real Time Streaming Protocol) with RTP for the actual streaming and RTCP for the control, but depending on the application, other network protocols can be more appropriate. Synchronization is also required between audio and video, or sometimes even between different correlated streams e.g. from multiple cameras. In addition, embedded systems often require customizations, e.g. proprietary protocols, hardware acceleration, and porting to specific chipsets.

Fortunately, there are free and open source multimedia streaming libraries that contain most of the software required for implementing multimedia streaming. For instance, both GStreamer and VLC include many optimized codecs and make use of hardware acceleration. They use much of the same codec libraries (e.g. FFMPEG, a highly optimized codec library including MPEG and H.264 coding and decoding, and FAAD, an AAC codec used for MPEG-4 audio). GStreamer also has an OpenMAX interface, which facilitates the integration of new hardware codecs. VLC includes both a library and an application, which makes it possible to prototype your own application without writing any code at all. In addition, the open source nature of these libraries allows you to add new features and fix issues according to your own agenda without having to depend on the road-map and priorities of a commercial third party.

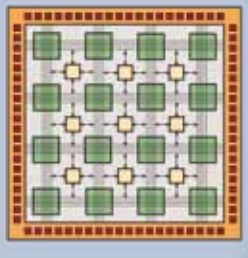
gstreamer

These libraries contain most software required to implement multimedia streaming, however they are not always so trivial to use correctly, especially on a first project. There are many typical pitfalls to be avoided and it is important to have experience in communicating with the main developers of these libraries for bug fixes and new features. That is why many companies decide to work with experts to guide them in this process and to help them take the right decisions at project start. The consultants of Mind are used to working with multimedia streaming technologies and they have implemented a number of applications based on VLC and GStreamer. This expertise can either allow companies to be quickly up and running on multimedia technologies, or at the contrary, to remove the burden of learning the details about the multimedia library, so that they can focus on their own added value and core expertise. ■

Ramses Valvekens, CEO of Easics NV, member of DSP Valley wrote a reply to Peter Simkens' column "The importance of DSP according to Forward Concepts", that was published in our previous newsletter n°2 (April-May 2009)

Hello Peter,

You are right. DSP is omnipresent. Common DSP-platforms are not only Digital Signal Processors, but also ASSPs/ASICs and MCUs/MPUs.
ASSPs/ASICs have even dwarfed the market share of traditional Digital Signal Processors. Mobile phones, with over 1 billion units shipped annually, all contain ASSPs as their baseband DSP-platform.
FPGAs are emerging as another DSP-platform. They have become competitive as the FPGA-vendors have aggressively scaled their devices down to 65 and even 40 nm.
FPGAs are flexible (almost like software), and can exploit massive parallelism. They contain up to tens or even hundreds of dedicated high-speed multiply-add blocks. This is a perfect fit for applications such as real-time industrial image and video processing.
Once power consumption and unit prices go further down, and application development will become more of a software programming job, they too will be embraced by consumer electronics manufacturers.



Regards,
Ramses Valvekens
(Easics NV)
ramses@easics.be

New director appointed for the DSP Valley network in the Netherlands

Already 30% of the DSP Valley members are located in the Netherlands. For sure it is time again to revive and grow the DSP Valley network in the Netherlands. Proximity between DSP Valley Eindhoven and the Dutch members is a condition to have a successful embedded systems community.

"I started last week and already enjoy working with the enthusiastic DSP Valley team", says Arthur Pouwels, new appointed director in Eindhoven. *"My experience lies with radar systems, GSM networks, mobile displays and audio/video signal processing, which I can use to build bridges between the several application domains."*

DSP Valley is asked by Point One to build an active embedded community with SME's, system integrators and knowledge institutes. Arthur will start making an overview of the Dutch players, who can participate in the Point-One Embedded System community and then he will make an inventory of their key issues. The end goal is of course, as DSP Valley is already doing for more than 12 years now, facilitating new innovative co-operation by organizing network events, technical lectures and B2B matchmakings.

"I am looking forward to meet the DSP Valley members and start building the embedded systems community."

Arthur has his office on the High Tech Campus in Eindhoven and can be contacted at the following coordinates:
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DSP Valley @ ESC Silicon Valley

From 30th March until 2nd April 2009 DSP Valley was present together with two of its members, IMEC and NXP Semiconductors at the Embedded Systems Conference Silicon Valley in the McEnery Convention Center in San Jose, CA (USA). ESC

It is the spring's largest gathering for system architects and design engineers that combines real time networking, innovations and training, all in one place. Now in its 21st year, ESC Silicon Valley offers the opportunity to see first hand how the electronic engineering industry is shaping our futures – through new technologies that will change global business and industry, and our daily lives.

The next edition will again take place in San Jose, CA (USA) from 26 until 29 April 2010.

DSP Valley @ ESEC 2009

For the seventh time in a row DSP Valley was present at the Embedded Systems Exhibition & Conference (ESEC) that was held from the 13th till the 15th of May 2009 at the 'Tokyo Big Sight' exhibition center in Tokyo (Japan). DSP Valley and the Flanders Investment & Trade (FIT) office in Tokyo joint forces to setup a group booth at this international event. The ESEC event concurrently ran with eight other IT related exhibitions. For the first time there was the Green IT exhibition gathering power-saving, environment-conscious products and solutions. ESEC is definitely the largest one of these 9 exhibitions as well in the total floor space as in the number of exhibitors. Almost 114.000 people registered for this year's edition.

DSP Valley, distinguishing itself as a center of excellence in DSP and embedded systems design, was present with four of its members: AnSem, ICsense, NXP Semiconductors and Target Compiler Technologies. The last company demonstrated their products also on the booth of their Japanese distributor Innotech. By its presence DSP Valley promotes the competences available in the network in the domain of designing embedded systems for signal processing.

On our booth we did not only receive people from the big Japanese electronics manufacturers and embedded software service companies but also representatives from distributors. People from more than eighty companies visited our booth and had discussions with the members. It was a great honor to have a visit of the Belgian ambassador on the first day of the exhibition. To get the visitor's contact information, most of the Japanese booths had nice looking Japanese ladies hunting for your business card in return for a gadget. On the DSP Valley group booth the visitors could not only visit the technology demonstrators but they could also enjoy Belgian beer and Belgian chocolates.

You find a wide variety of exhibitors at ESEC. Manufacturers of all kinds of microprocessors, DSPs, Board computers, FPGAs, connectivity modules… On the software side we see provid-

Embedded Award 2009

Express Logic, Inc., the worldwide leader in royalty-free real-time operating systems (RTOS), was selected as the winner of the prestigious "Embedded AWARD 2009" at Embedded World. In selecting Express Logic for the AWARD in the tools category, the Embedded World selection committee judged BenchX as best among all new tools for embedded development. An independent jury of experts selected Express Logic's BenchX® as the best product in the tools category for its outstanding technical innovation in embedded technology.

BenchX is an Eclipse-based Integrated Development Environment (IDE) for embedded systems. It includes a project builder, text editor, C/C++ compiler, debugger, simulator, and a hardware debug probe. BenchX is customized and optimized for embedded development, representing significant enhancements and comprehensive integration into a polished commercial product. BenchX is designed to support development based on a variety of popular 32-bit microprocessor architectures. ■

expresslogic

embedded AWARD 2009

ers of EDA tools, companies providing development support tools, companies selling software products like RTOSes, embedded internet tools, software IP… Despite the international label, the exhibition is mainly focused on the Japanese market since we see little non-Japanese exhibitors.

For a non-Japanese visitor it is often frustrating that the language barrier is very tough. Therefore the collaboration with a local distributor or representative is very valuable to tackle the language barrier. Thanks to the excellent organization and support of the local FIT staff the DSP Valley members had a very good exhibition participation.

The next edition of ESEC will take place at the same place in Tokyo from 12th till 14th May 2010. ■

Advanced Concepts for Intelligent Vision Systems - Acivs 2009

http://acivs.org/acivs2009/

Organized by the SEE
Mercure Chateau Chartrons,
Bordeaux, France
September 28 - October 2, 2009

Acivs 2009 is a conference focusing on techniques for building adaptive, intelligent, safe and secure imaging systems. Acivs 2009 consists of four days of lecture sessions, both regular (25 mns) and invited presentations, poster sessions and a special session on performance assessment of vision systems. The proceedings of Acivs 2009 will be published by Springer Verlag in the Lecture Notes in Computer Science series and are listed in the ISI conference proceedings citation index.

Acivs 2009 will feature a conference dinner, and other social activities.

The conference fee includes the social program (conference dinner, opening reception, and cultural activities), coffee breaks, daily lunches and a hard-copy of the proceedings. Students, IEEE and SEE members can register at a reduced fee.

Contact Information

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